

Technology Offer

Globally synchronous electronic clocks based on networks of mutually delay-coupled phase-locked loops

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Abstract

Mutually delay-coupled phase-locked loops (PLLs) enhance network synchronization by leveraging the self-organization dynamics of interconnected nodes each outfitted with controllable oscillators. These systems ensure stable in-phase locking of spatially distributed oscillators in the presence of considerable signaling time-delays and thereby provide precise clocking signals, e.g., essential for high precision localization services. The scalability and robustness of self-organized synchronization has been shown in many experiments and a model allows to predict the properties of synchronization qualitatively and quantitatively.

Advantages

- **Robustness:** If one part of such a decentralized and yet coordinated network fails, the remainder of the network is not affected and remains functional.
- **High accuracy:** Enables real-time synchronization with picosecond accuracy.
- **Decentralized Security:** Immune to spoofing and spamming as there is no central communication path that could be interfered with any and an attack would be detectable throughout the system.

Potential applications

- **Power Grid:** Less vulnerable and costly than current GPS-based solutions, while maintaining real-time synchronization.
- **Satellite Coordination:** Elimination of Master-Slave systems; time synchronization is possible without ground stations.
- **Precision Agriculture:** Synchronizing of autonomous machines and steering systems of fast-moving entities with high accuracy field navigation.
- **Warehouse Automation:** Specific localization of goods and faster synchronization of automated robots, while working under extreme conditions.
- **Scalability:** Easy scale up as there is no need for a communication infrastructure.

Background

Traditional network synchronization methods are usually realized by hierarchical entrainment of electronic clocks using a dedicated and precise reference oscillator (Fig. 1, left). However, this conventional approach has its limitations, such as phase error accumulation and increasingly complex design constrains as the system size grows. Self-organized synchronization for electronic networks has been considered since 1980s. However, until now, no robust mathematical model was available to predict the properties of self-organizes synchronous states in the presence of considerable time-delays. The novel model offered here enables the architectural design of self-organizes synchronization hardware.

Technology

The core innovation lies in the network's architecture, where each node is equipped with a digitally controlled phase-locked loop (PLL). These PLLs are interconnected in such a way that they can synchronize their clocks through a self-organizing mechanism in a decentralized manner (Fig. 1, right). The system dynamically adjusts the phase and frequency of each node's oscillator based on the collective behavior observed through the network, ensuring that all nodes achieve and maintain precise timing alignment in the presence of considerable signaling time-delay, as well as physical and operational variances. Thus, the presence of signaling time-delays does not introduce phase-shifts between the oscillators, resulting in more precise synchronization. Fig. 2 shows a photograph of such a 24 GHz PLL node connected to a delay board, allowing to tune the time delay for experimental validation.

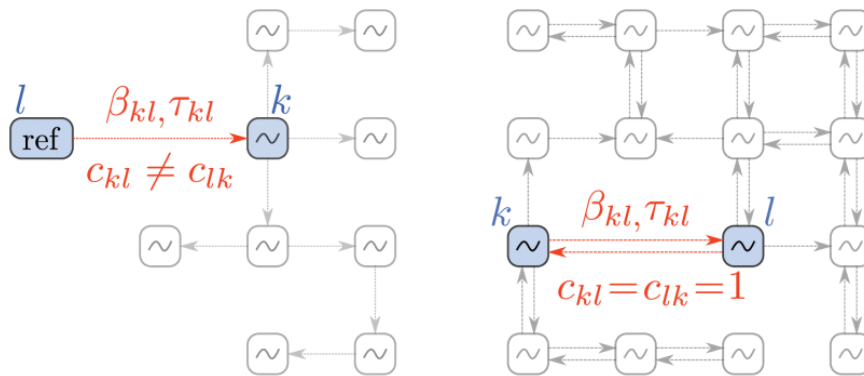


Figure 1: Left: Hierarchical clock tree network structure with reference oscillator. Right: Mutual coupling network structure without reference oscillator.

τ : cross-coupling time delay; c_{kl} or c_{lk} components of the network's adjacency matrix being either one if there is a connection from PLL l to k or k to l or zero otherwise; β : phase offset of oscillator

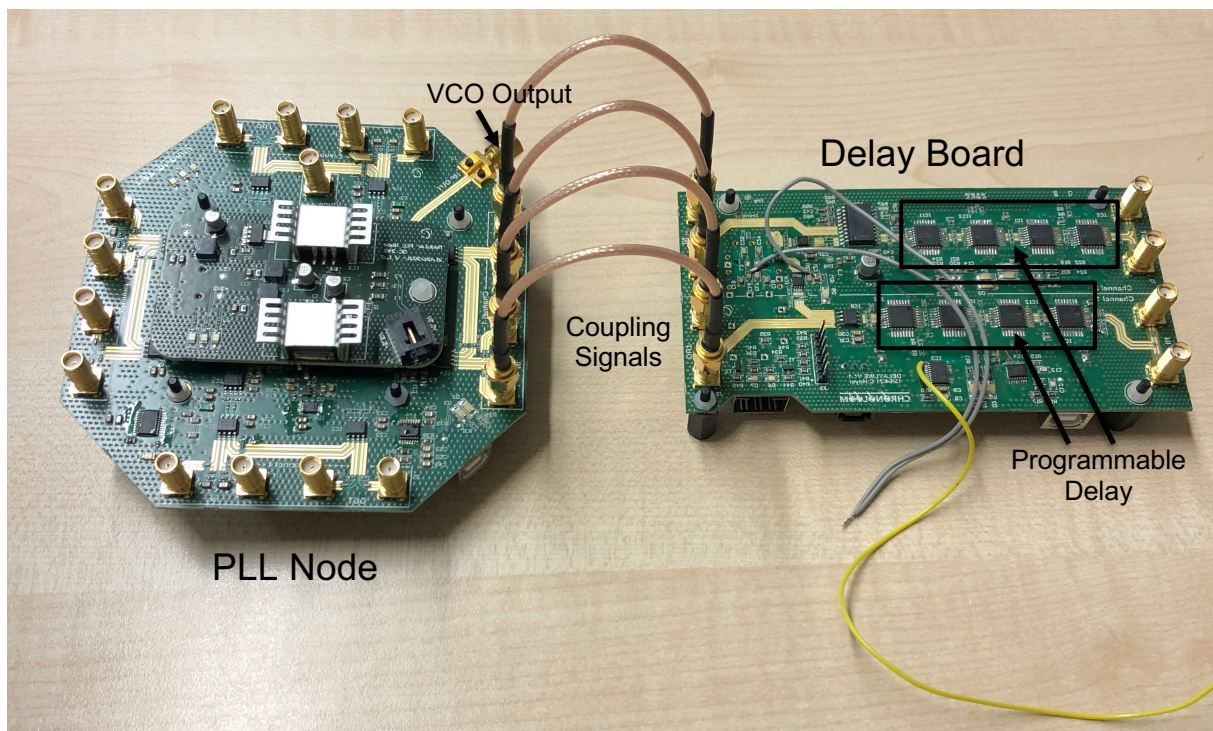


Figure 2: Photograph of a fully assembled PLL node with four in- and output channels connected to the delay board, whereas VCO describes the voltage-controlled oscillator and PD the phase detector. The size of this PLL node board is 121 mm x 121 mm and the size of the delay board is 136 mm x 72 mm.

Conducted Experiments

- Stability of synchronized states in networks of delay-coupled oscillators was theoretically analyzed and validated. The stability criteria were derived considering time delays and inertia in relation to coupling strength, time delay, damping, and inertia.^[1]
- Demonstrated that parameter heterogeneity stabilizes synchronization in a network of 24 GHz oscillators. Networks of PLLs with varying coupling strength and intrinsic frequencies were tested.^[2]



- Achieved mutual synchronization of 24 GHz PLL oscillators over distances up to 500 m with time delays up to 2.5 ms. The results show that synchronization over these distances is possible without additional infrastructure, potentially lowering implementation costs in certain scenarios.^[3]
- Verified synchronization of two bidirectionally coupled 24 GHz PLL systems for time delays up to 14 ns. VCO output frequencies around 24.25 GHz, synchronization observed at division factors (N=512, 128, 32), with time delays ranging from 4.24 ns to 14.48 ns.^[5]

Patent Information

PCT application WO2015193512A1 filed on 22.06.2015, EP2957982B1, CN106462177B and US10241539B2 granted; KR102029320B1 and TWI721948B application.

Publications

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[3] C. Hoyer, L. Wetzel, D. Prousalis, J. Wagner, F. Jülicher, F. Ellinger, "Mutual Synchronization of Spatially Distributed 24 GHz Oscillators up to Distances of 500 m", IEEE Transactions on Circuits and Systems II: Express Briefs 69(9), 3689, 2022 [10.1109/TCSII.2022.3176827](https://doi.org/10.1109/TCSII.2022.3176827).

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[5] C. Hoyer, D. Prousalis, L. Wetzel, R. Riaz, J. Wagner, F. Jülicher, F. Ellinger, "Mutual Synchronization with 24 GHz Oscillators", International Symposium on Circuits and Systems (ISCAS), 1, 2021, <https://ieeexplore.ieee.org/abstract/document/9401555>.

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